
80V Input, 100mA Output Current, Low Quiescent Current LDO



SCT71801A00Q Series

Orderable Device	Output Voltage	Package	Package Marking	PINS	MSL	Transport Media, Quantity
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PARAMETER	DEFINITION	MIN	MAX	UNIT

PARAMETER	DEFINITION	MIN	MAX	UNIT

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PARAMETER	THERMAL METRIC	EMSOP-8L	UNIT
(1)			
(2)			
R JA_EVM(3)			

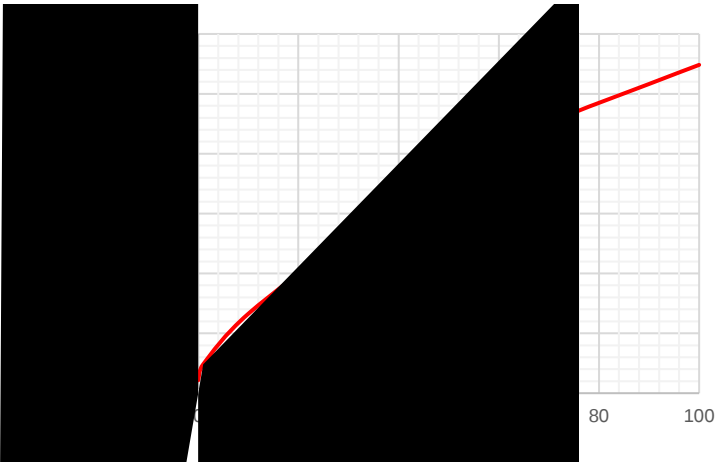
- (1)
- (2)
- (3)

[illegible][illegible]

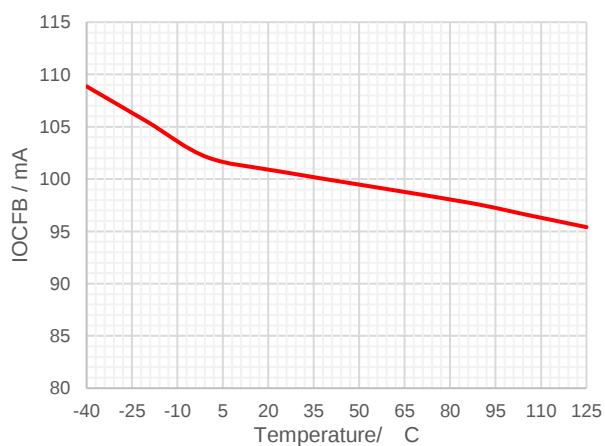
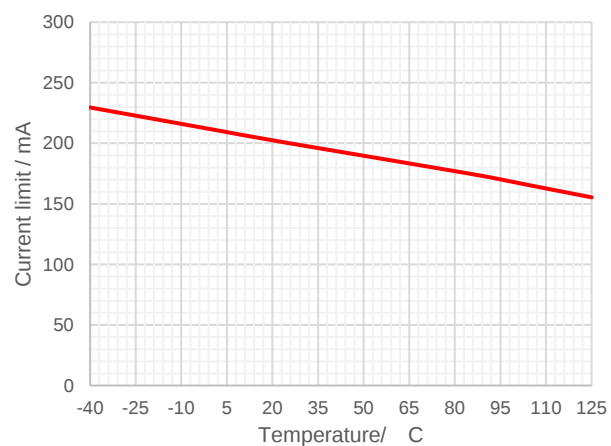
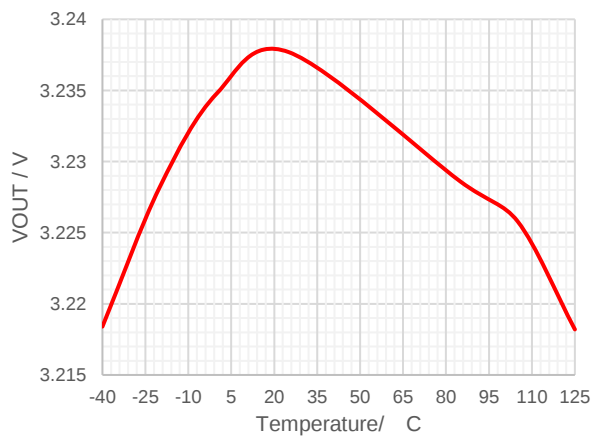
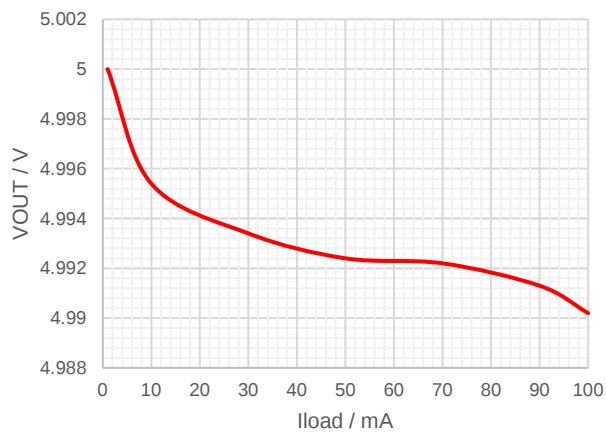
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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		= VPG_LOW /0.1mA				
Thermal Protection						

- (1)
- (2)
- (3)
- (4)



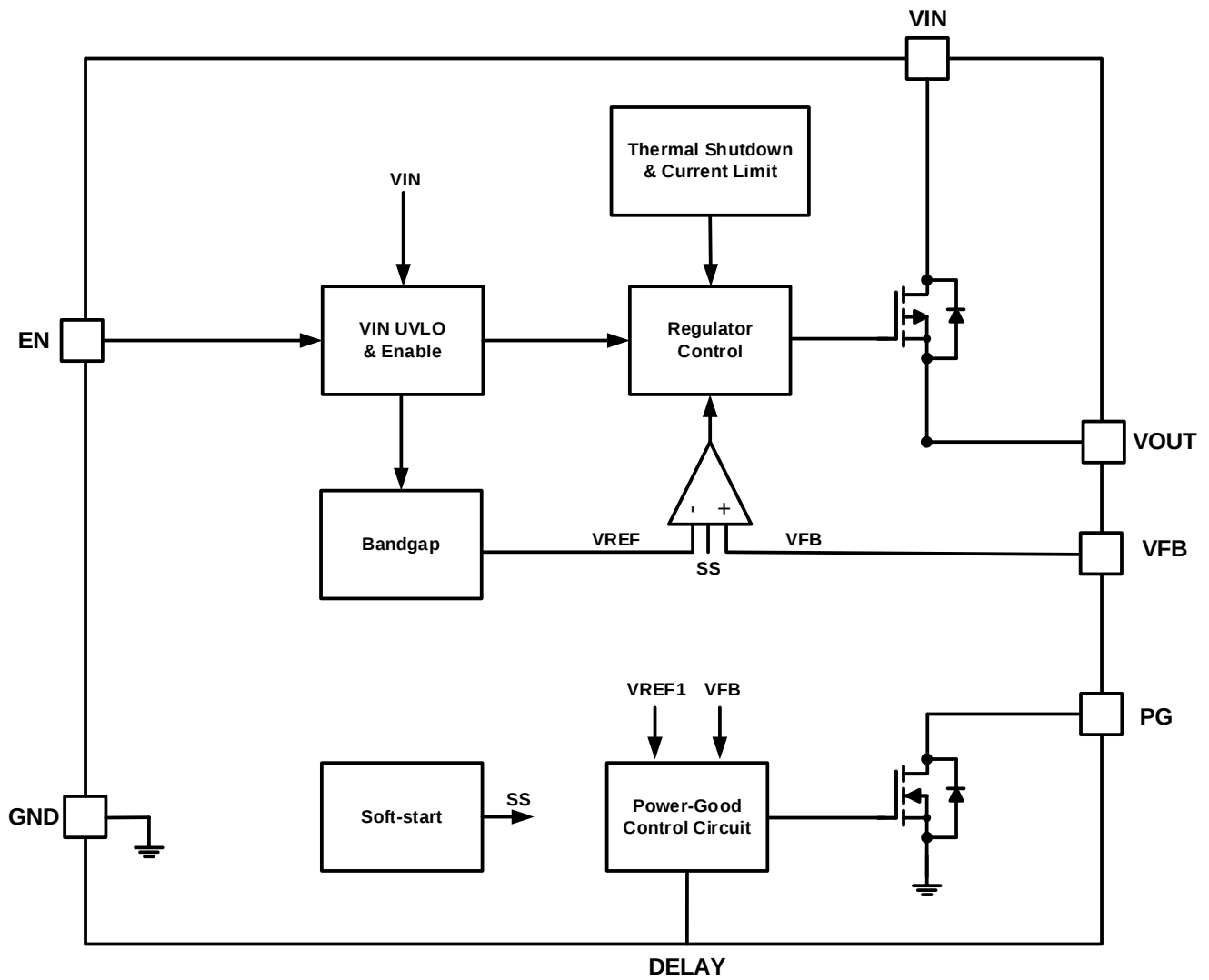
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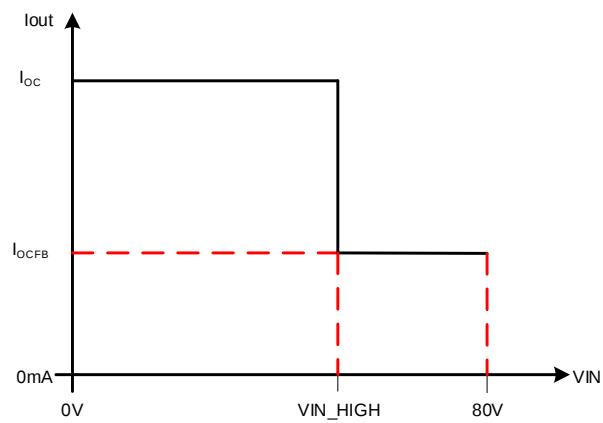


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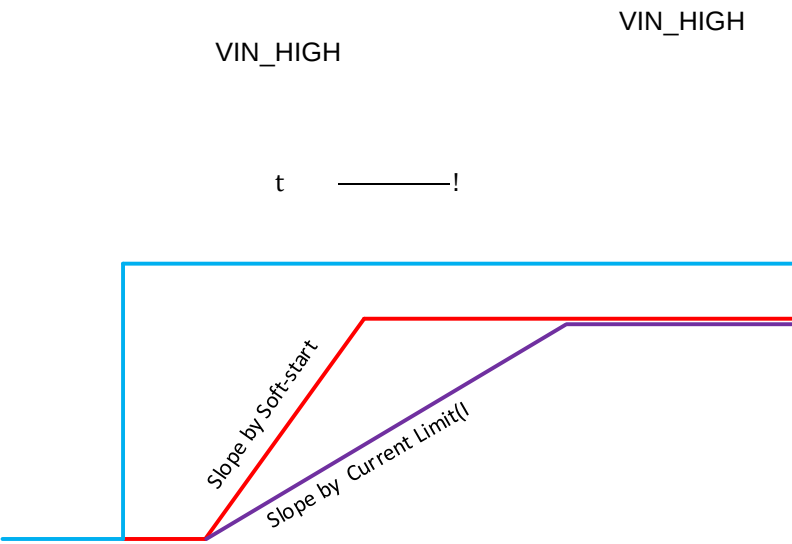
Overview

Enable and Under Voltage Lockout Threshold

VIN_HIGH Control



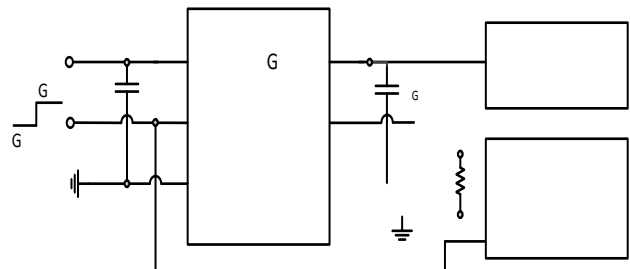
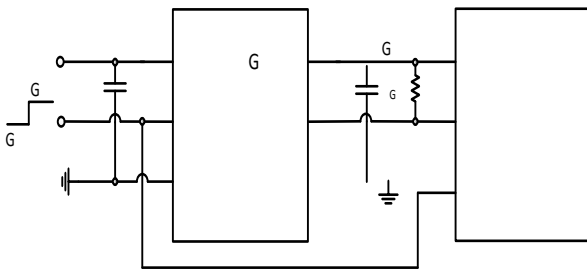
Internal Soft-Start

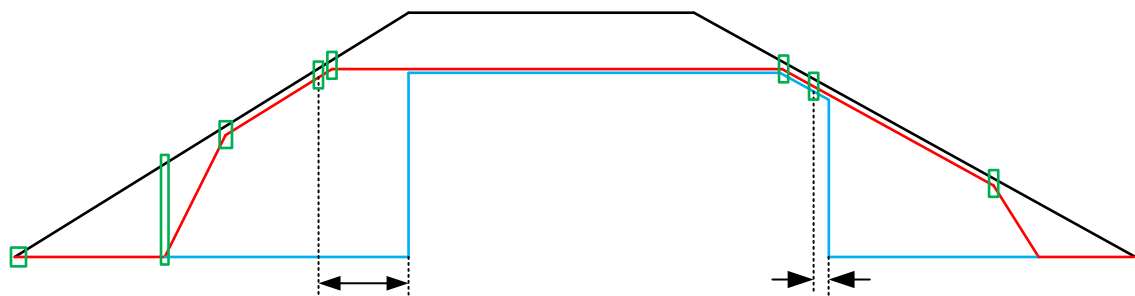


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Power-Good and Power-Good Delay

When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT} , and V_{DELAY} exceeds V_{REF} . The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when $C_{DELAY} = 10 \text{ nF}$, the PG delay time is approximately 12 ms; that is, $(10 \text{ nF} \times 1.2\text{V}) / 1\mu\text{A} = 12 \text{ ms}$.

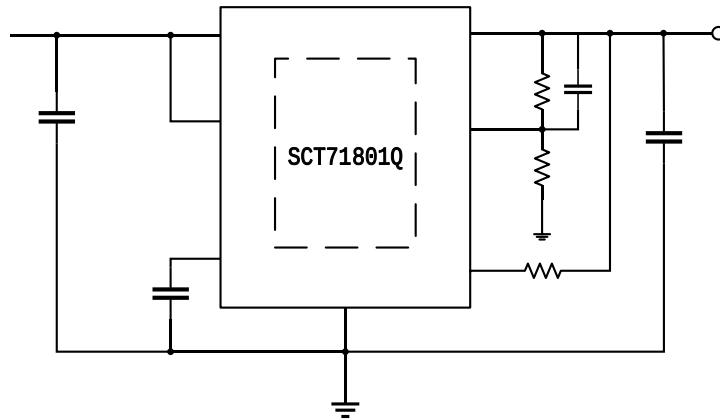




Thermal Shutdown

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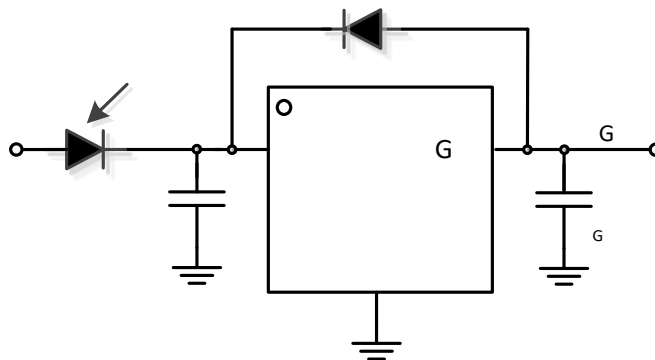
Typical application 1:



Design Parameters

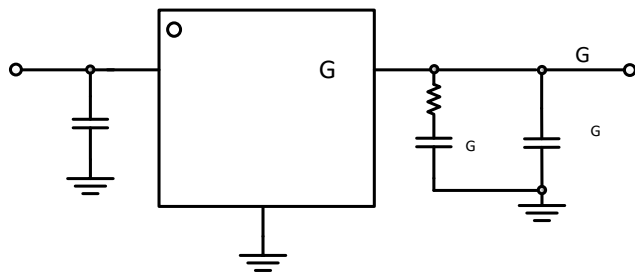
Design Parameters	Example Value

Typical application 2:



Design Parameters	
Design Parameters	Example Value

Typical application 3:



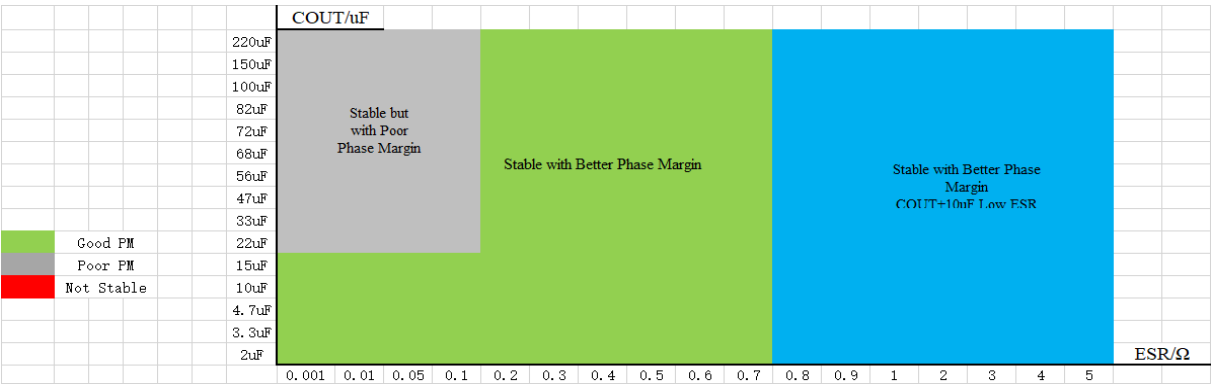
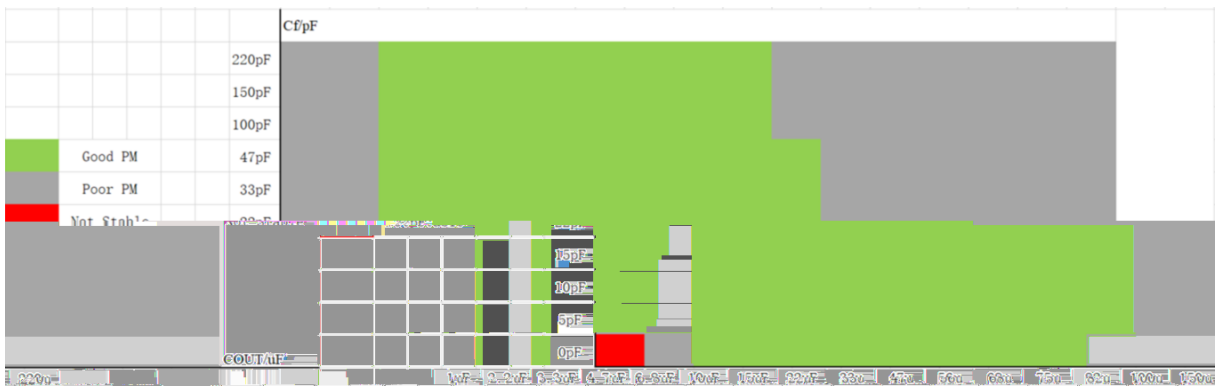
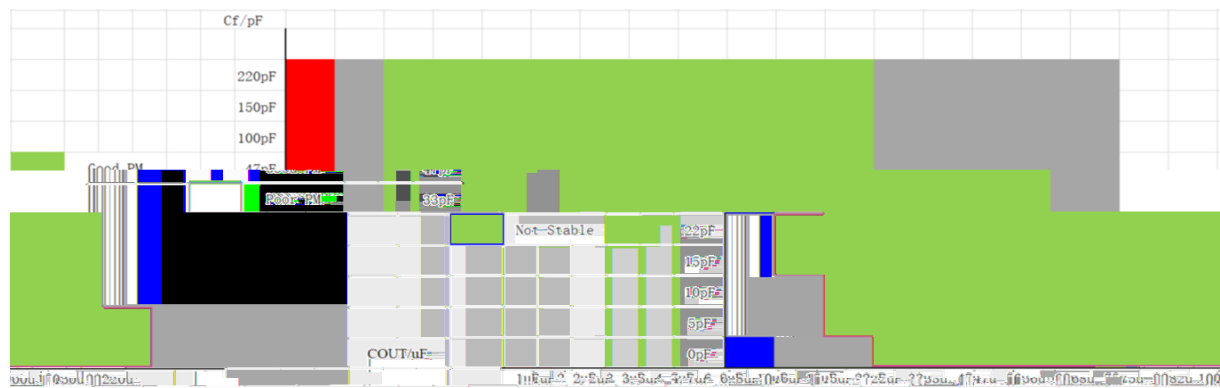
Design Parameters	
Design Parameters	Example Value

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Output Voltage

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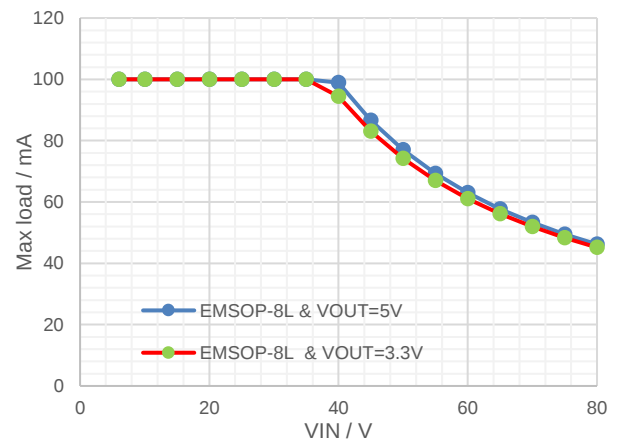
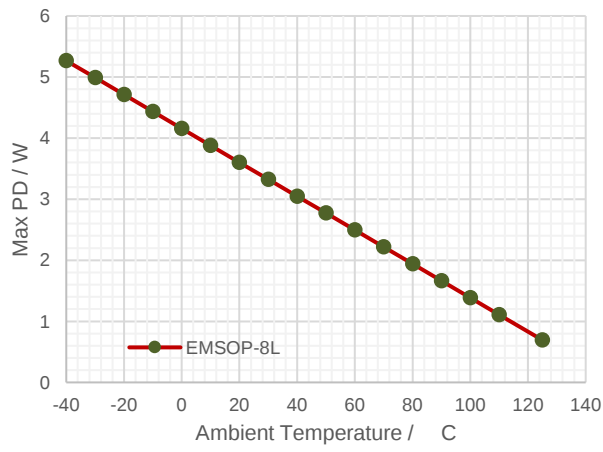
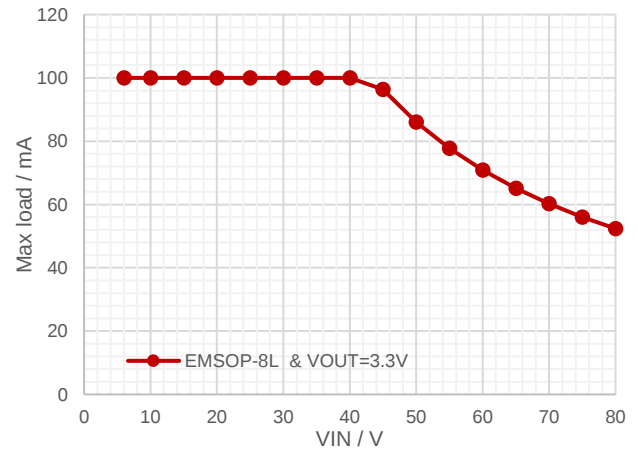
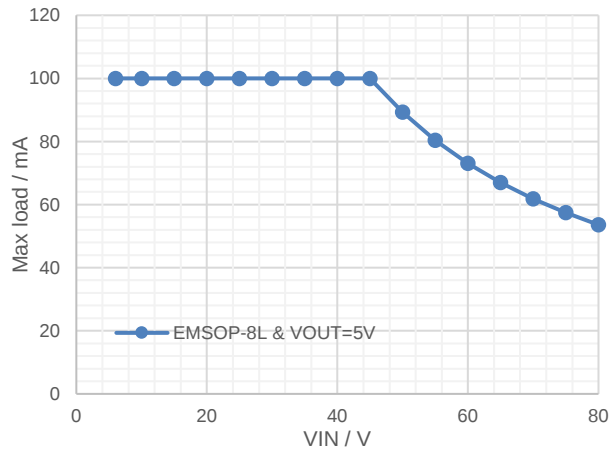
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Power Dissipation and Thermal Performance

Thermal Performance of Different Packages Based on EVM Test

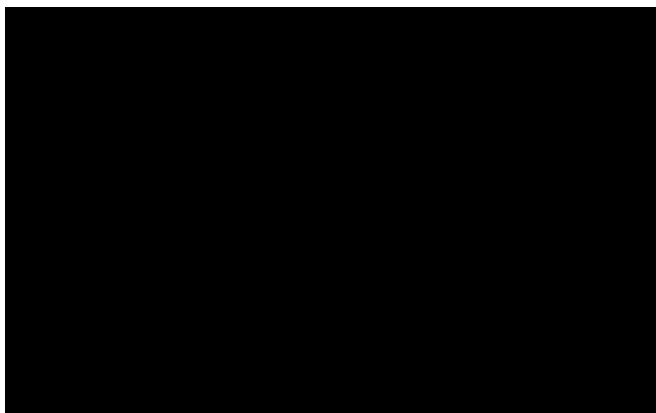
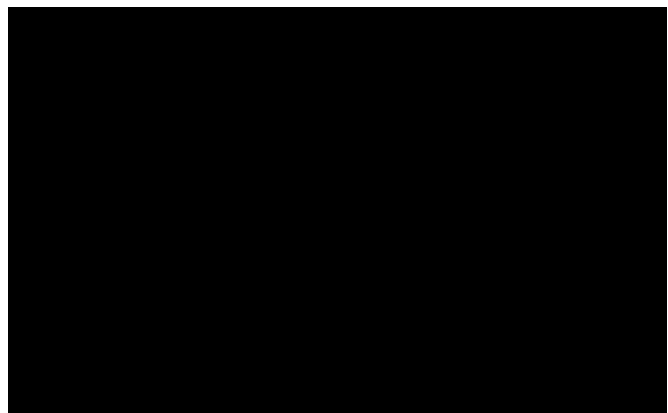
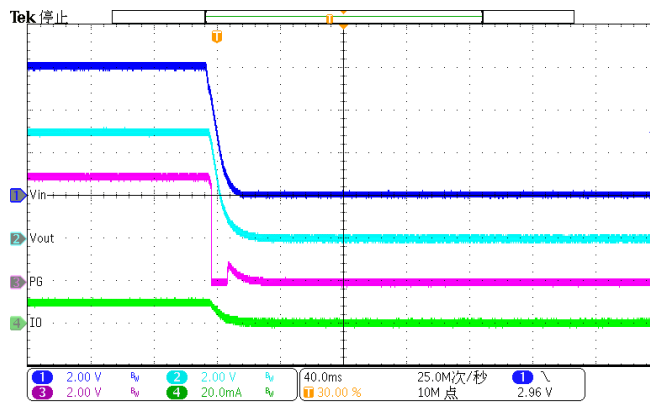
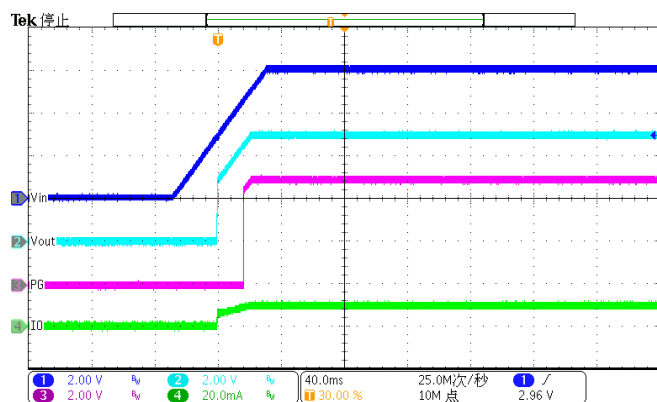
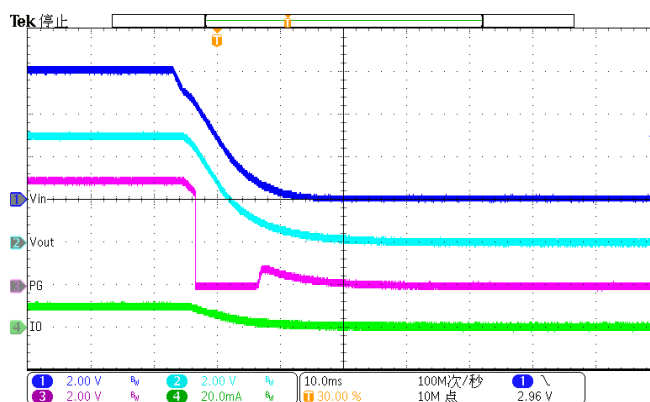
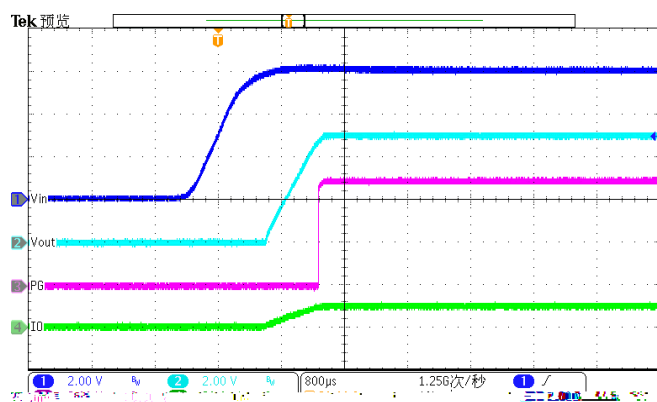
Package	Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)	Max Allowable PD (W) (TJ≤150)	R _{JA_EVM} (°C/W)

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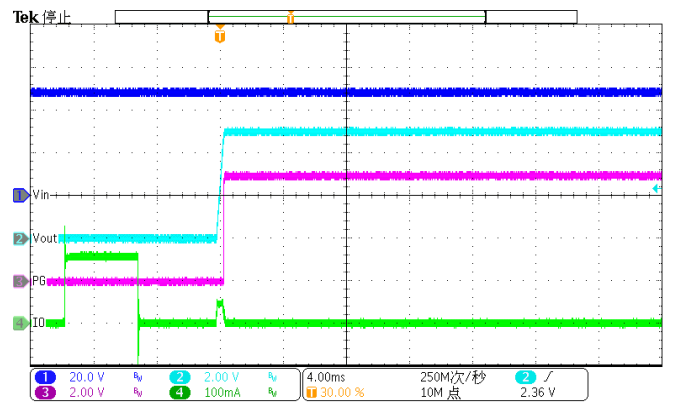
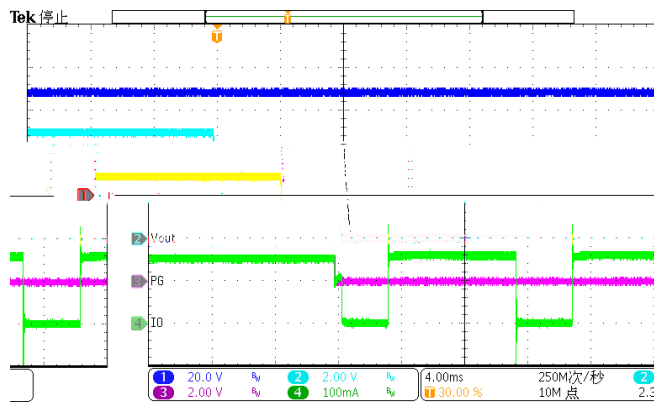
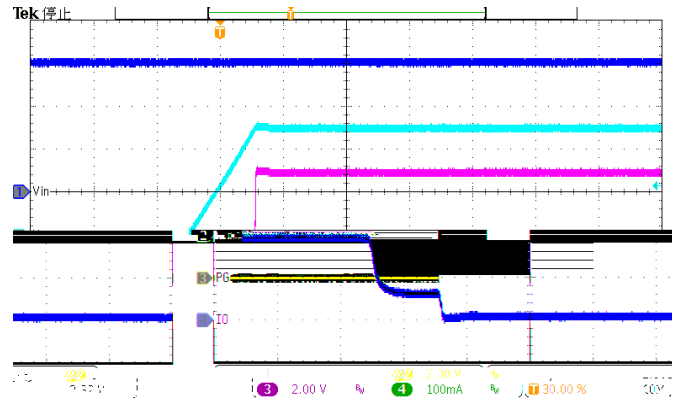
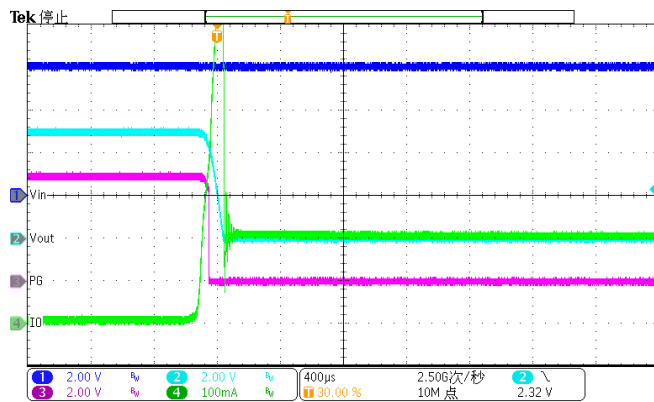
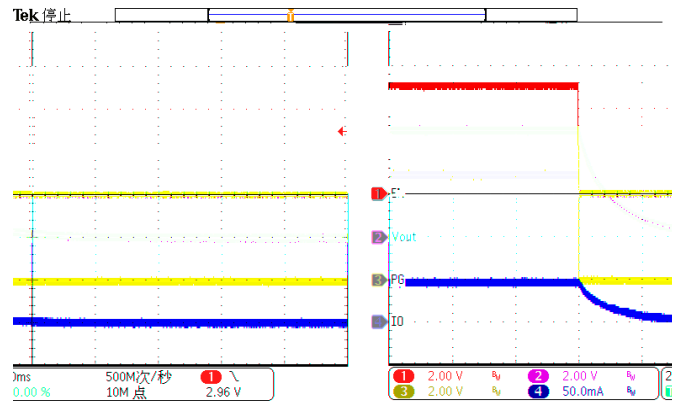
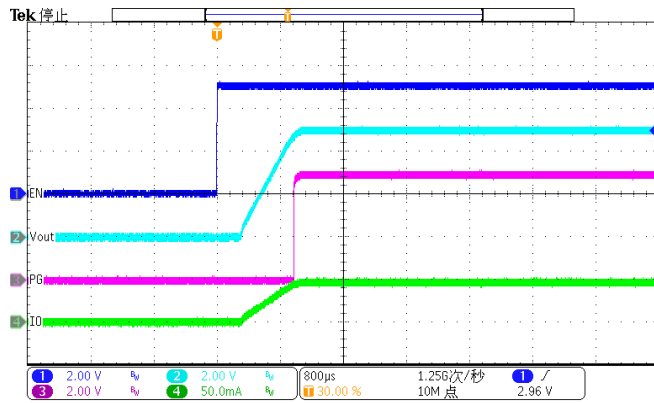


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Application Waveforms



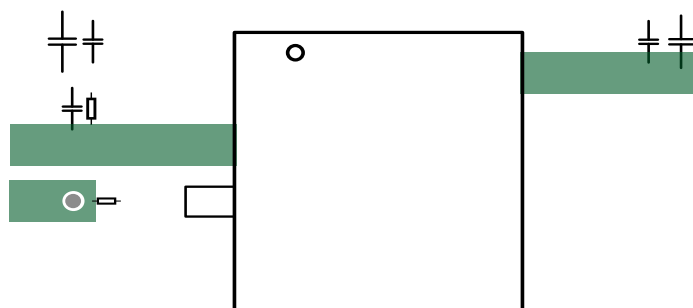
Application Waveforms(Continued)



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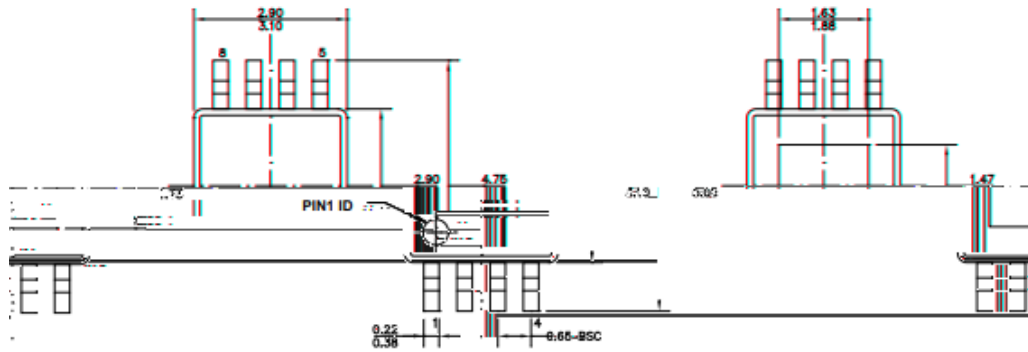
Layout Guideline

- 1.
- 2.
- 3.
- 4.
- 5.



SCT71801A00QMTER

PACKAGE OUTLINE DRAWING FOR MSOP8L-EP POD-0050 Revision 0.0



TOP VIEW

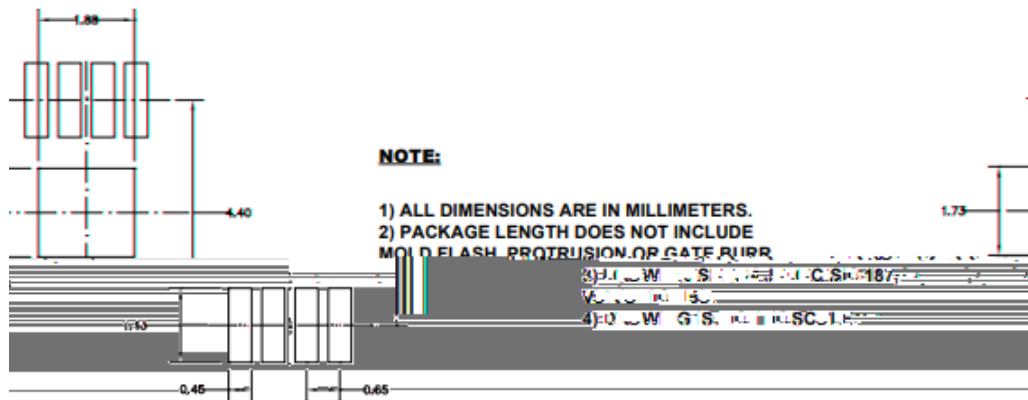
TOP VIEW

BOTTOM VIEW



FRONT VIEW

SIDE VIEW

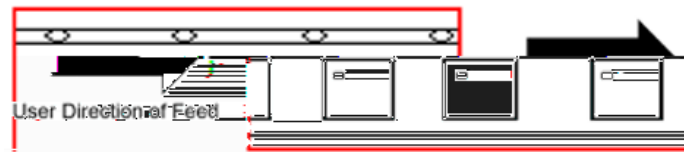
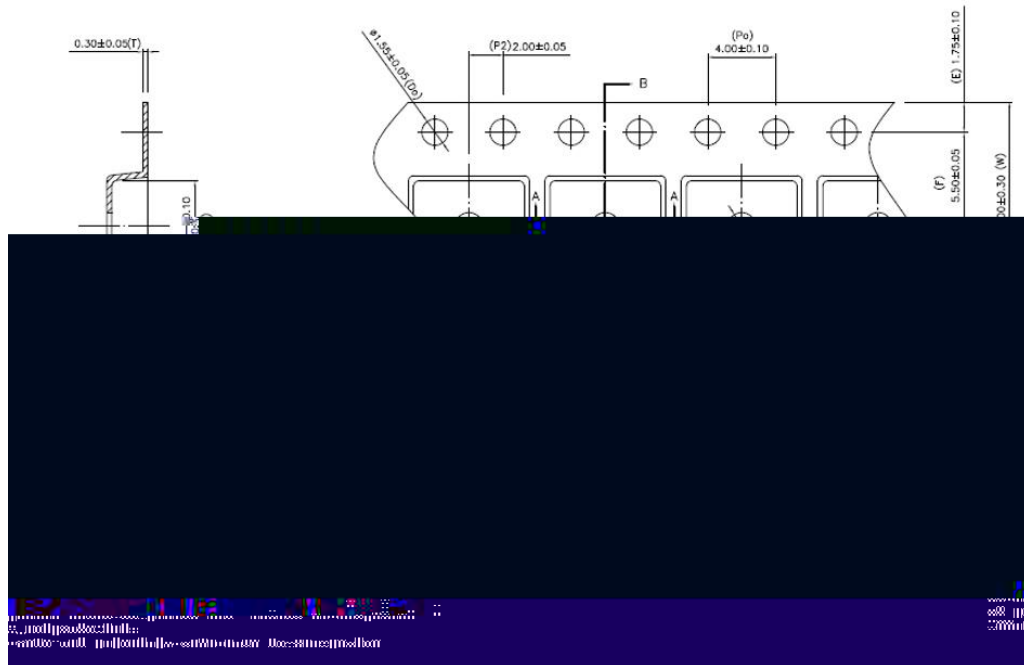
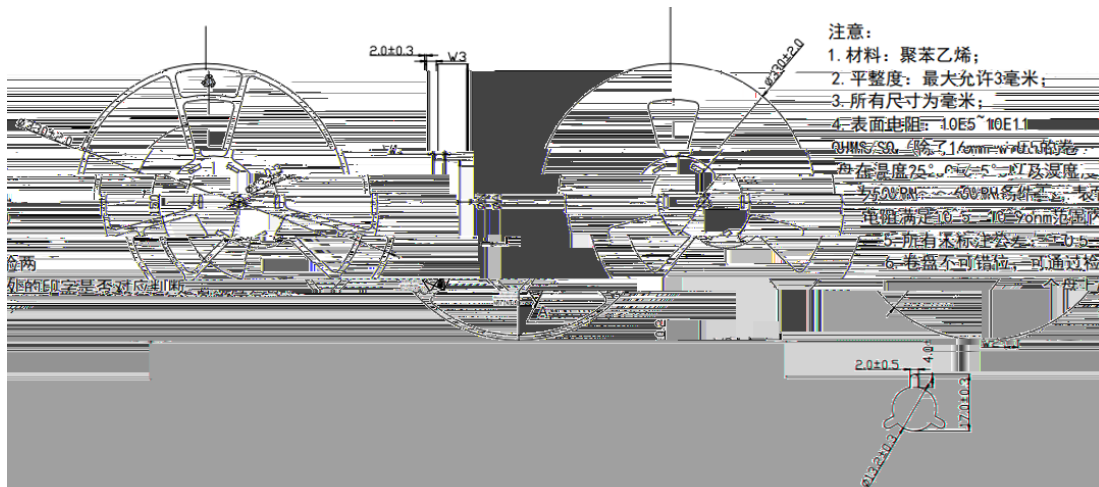


RECOMMENDED LAND PATTERN

NOTE:

- 1.
- 2.
- 3.
- 4.
- 5.
- 6.

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NOTICE: