4.1-40V 160-mΩ Quad-Channel Smart High-Side Switch

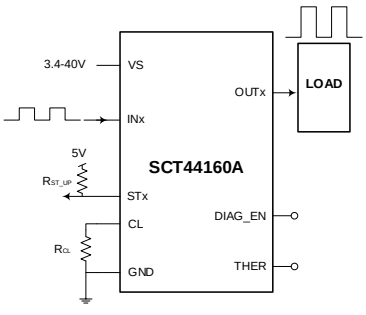
- Quad-Channel 160-mΩ Smart High-Side Switch With Full Diagnostics
  - A Version: Open-Drain Digital Output
  - B Version: Current Sense Analog Output
  - C Version: Current Sense Analog Output +4 CL pin for each channel
- Wide Operating Voltage: 4.1 V to 40 V
- High accurate current sense: ±15% @ 500mA, ±30% @ 50mA with B Version and C Version
- Adjustable current limit: ±30% when > 250mA, ±15% when > 500mA
- Protection:
  - Short-to-GND Protection by Current Limit (Internal or External)
  - Thermal Shutdown With Latch-Off Option and Thermal Swing
  - Inductive Load Negative Voltage Clamp with Optimized Slew Rate
  - Loss-of-GND and Loss-of-Battery Protection
- Diagnostic:
  - Overcurrent and Short-to-Ground Detection
  - Open Load / Short to Battery Detection During On and Off State
  - Global Fault Report for Fast Hardware Interrupt
- Available in an ETSSOP-28L Package
- High-Side Relay Drivers
- Power Switch for Sub-Module Power Supply
- Low Wattage Lamp Power Switch
- General Resistive, Inductive, and Capacitive Loads

The SCT44160 device is fully protected quad-channel smart high-side switch with four integrated 160-mΩ NMOS power FETs.
For version A, the device implements the digital fault report with an open-drain structure, Quad channel synchronous setting of current limit value.

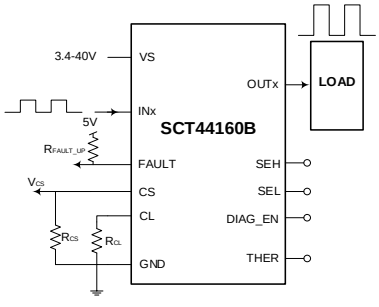
For version B, the device achieves high-precision current detection, making diagnosis more accurate, Quad channel synchronous setting of current limit value.

For version C, the device can achieve high-precision current detection while setting current limits for each channel separately.

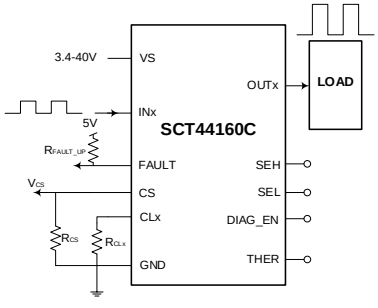
The SCT44160 provides current limit, thermal shutdown protection. Full diagnostics and high-accuracy current sense enable intelligent control of the load. The device is available in a 28-pin ETSSOP-28 package.



Typical Application of Version A



Typical Application of Version B



Typical Application of Version C

Revision 1.0: Released to market

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT44160AMZER	Tape & Reel	4000	160A	28	ETSSOP-28L	3
SCT44160BMZER	Tape & Reel	4000	160B	28	ETSSOP-28L	3
SCT44160CMZER	Tape & Reel	4000	160C	28	ETSSOP-28L	3

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VS (t < 400 mS)	-0.3	45	V
Reverse polarity voltage	-36		V
Current on GND (t < 2 minutes)	-100	250	mA
Voltage on INx, DIAG_EN, SEL, SEH, and THER	-0.3	7	V
Current on INx, DIAG_EN, SEL, SEH, and THER	-10		mA
Voltage on STx or FAULT	-0.3	7	V
Current on STx or FAULT	-30	10	mA
Voltage on CS	--2.7	7	V
Current on CS		30	mA
Voltage on CL, CL1, CL2, CL3, CL4	-0.3	7	V
Current on CL, CL1, CL2, CL3, CL4		6	mA
Inductive load switch-off energy dissipation, single pulse, single channel		40	mJ
Junction temperature(2)	-40	150	C
Storage temperature T_{STG}	-65	150	C

NAME	NO.			I/O(1)	PIN FUNCTION
	A Version	B Version	C Version		
GND	1,12	1,12	1,12	G	IC ground pin.
NC	2,19,24	2,19,24	-	-	Not Connection.
CL1	-	-	2	O	Adjustable the current limit of channel 1.
		3	3		Channel 1 logic input, internal pulldown.
IN2	4	4	4	I	Channel 2 logic input, internal pulldown.
IN3	5	5	5	I	Channel 3 logic input, internal pulldown.
IN4	6	6	6	I	Channel 4 logic input, internal pulldown.
ST1	7	-	-	O	Open-drain diagnostic status output for channel 1, external pull-up voltage required.
ST2	8	-	-	O	Open-drain diagnostic status output for channel 2, external pull-up voltage required.
ST3	9	-	-	O	Open-drain diagnostic status output for channel 3, external pull-up voltage required.
ST4	10	-	-	O	Open-drain diagnostic status output for channel 4, external pull-up voltage required.
SEH	-	7	7	I	CS channel-selection high bit; internal pulldown.
SEL	-	8	8	I	CS channel-selection low bit; internal pulldown.
FAULT	-	9	9	O	Global fault report with open-drain structure, ORed logic for quad-channel fault conditions.
CS	-	10	10	O	Current-sense output
CL	11	11	-	O	Adjustable current limits for quad channels
CL4	-	-	11	O	Adjustable the current limit of channel 4.
THER	13	13			

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{VS}	Input voltage range	4.1	40	V
INx, DIAG_EN, SEL, SHE,THER	External pull-up voltage range	0	5	V
STx, FAULT	External pull-up voltage range	0	5	V
Nominal dc load current		0	1.5	A
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, VS pins(1)	-1	+1	kV
	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, other pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

PARAMETER	THERMAL METRIC	ETSSOP-28L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	24.27	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	32.11	
$R_{\theta JC\ (bot)}$	Junction to case (bottom) thermal resistance(1)	2.49	
$R_{\theta JB}$	Junction to board thermal resistance(1)	9.17	
$R_{\psi JT}$	Junction-to-top characterization parameter	2.96	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT44160 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT44160. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 125°C ambient temperature range unless otherwise stated. VS = 13.5 V, INx = 5 V unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{VS}	Operating input		4.1		40	V
V_{VS_UVLO}	Input UVLO Threshold	V_{VS} rising		3.8	4.05	V
	Hysteresis			500		mV
I_{Q_OP}	Operating input current	DIAG_EN=5V,I_{OUTx}=0.5A, Current limit=2A,All channels on A version and B version		7.5		mA
		DIAG_EN=5V,I_{OUTx}=0.5A, Current limit=2A,All channels on C version		9.5		
I_{OFF}	Standby current	INx=DIAG_EN=THER=0V, CL=CS=Floating			0.3	uA
		INx=DIAG_EN=THER=0V, CL=CS=Floating,TJ=125℃			3	uA
$I_{OFF(DIAG)}$	Standby current with diagnostic enabled	INx=THER=0V,DIAG_EN=5V, VS-OUTx>V_{OL_OFF}		1	5	mA

Logic Input(INx,DIAG_EN,THER,SEH,SEL)					
V_{IH}	Logic high-level voltage		1.35	1.55	V
V_{IL}	Logic low-level voltage				

I_{CS_H}	Current-sense pin output current	V_{CS} =4.5V	10	22		mA
I_{CS_LKG}	Current-sense leakage current in disabled mode	DIAG_EN=0V,TJ=125℃			0.5	uA
Switching						
t_{D_ON}	Input to output propagation delay, Rising	DIAG_EN=5V, I_{OUTx} =0.5A, INx rising edge to 10% of V_{OUTx}		30		uS
t_{D_OFF}	Input to output propagation delay, Falling	DIAG_EN=5V, I_{OUTx} =0.5A, INx falling edge to 90% of V_{OUTx}		8		uS
V/ $t_{\_ON}$	Turnon slew rate	DIAG_EN=5V, I_{OUTx} =0.5A, V_{OUTx} from 10% to 90%		0.35		V/uS
V/ $t_{\_OFF}$	Turnoff slew rate	DIAG_EN=5V, I_{OUTx} =0.5A, V_{OUTx} from 90% to 100%		0.4		V/uS
t_{D_MATCH}	t_{D_RISE} - t_{D_FALL}			20		uS
Current Sense timing						
$t_{CS\_ON(EN)}$	CS settling time from DIAG_EN disabled	I_{OUTx} =0.5A, DIAG_EN rising edge to V_{CS} rising		3	10	uS
$t_{CS\_OFF(EN)}$	CS settling time from DIAG_EN enabled	I_{OUTx} =0.5A, DIAG_EN falling edge to V_{CS} falling		2	10	uS
$t_{CS\_ON(IN)}$	CS settling time from IN rising edge	DIAG_EN=5V, I_{OUTx} =0.5A, INx rising edge to V_{CS} rising		100	160	uS
$t_{CS\_OFF(IN)}$	CS settling time from IN falling edge	DIAG_EN=5V, I_{OUTx} =0.5A, INx rising edge to V_{CS} rising		3	10	uS
t_{SEx}	Multi-sense transition delay from channel to channel	DIAG_EN=5V,Current sense output delay when multi-sense pins SEL and SEH transition from channel to channel		100		uS

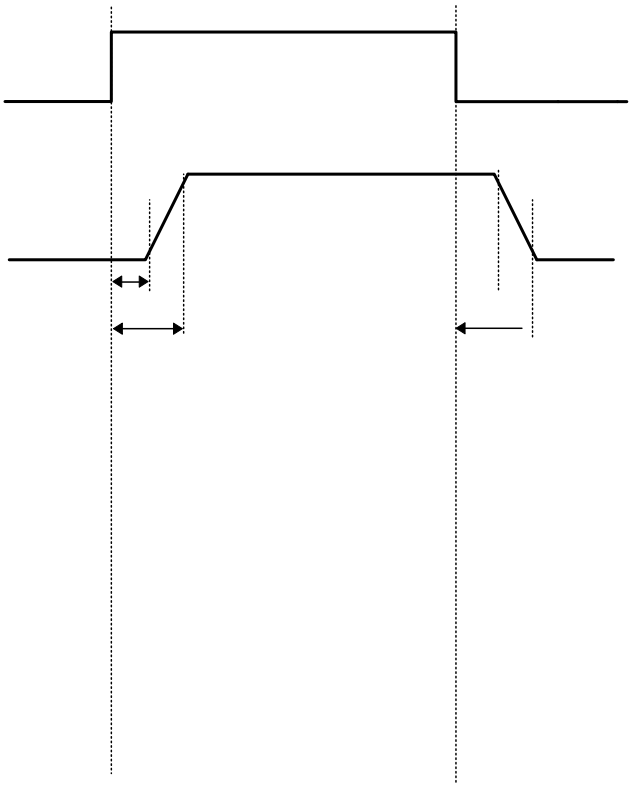


Figure 1. Output And CS Delay Sequential

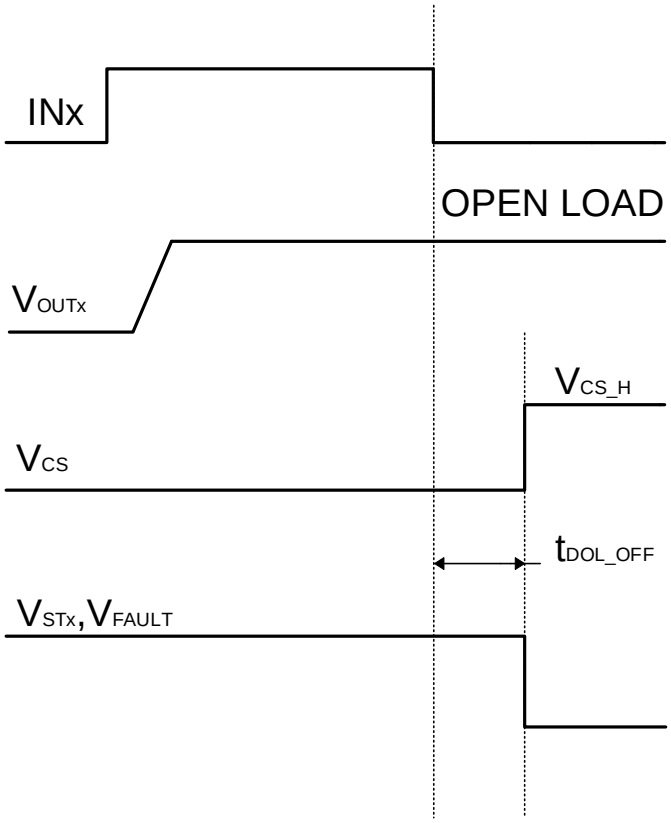


Figure 2. Open Load Delay

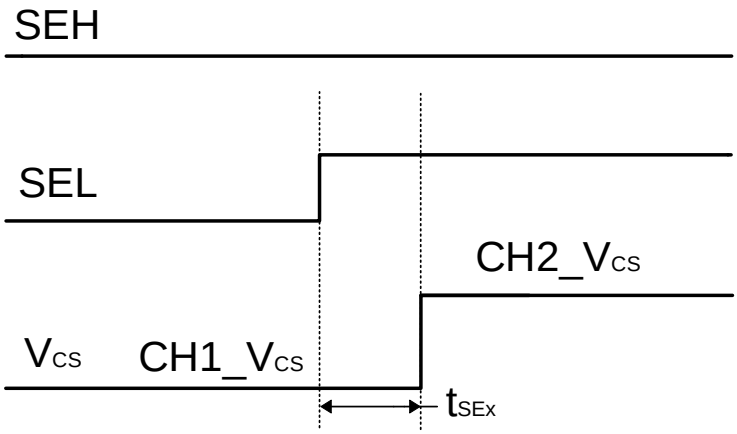


Figure 3. Multi-Sense Transition Delay

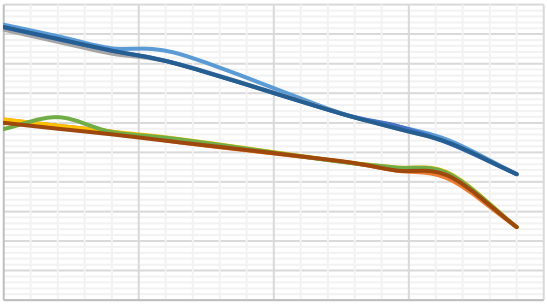


Figure 4. INx Threshold VS Temperature

Figure 5. DIAG_EN Threshold VS Temperature

Figure 6. Drain-to-Source Clamp Voltage VS Temperature

Figure 7. Body-Diode Forward Voltage VS Temperature

Figure 8. Channel-1 FET On-Resistance VS Temperature

Figure 9. Channel-2 FET On-Resistance VS Temperature

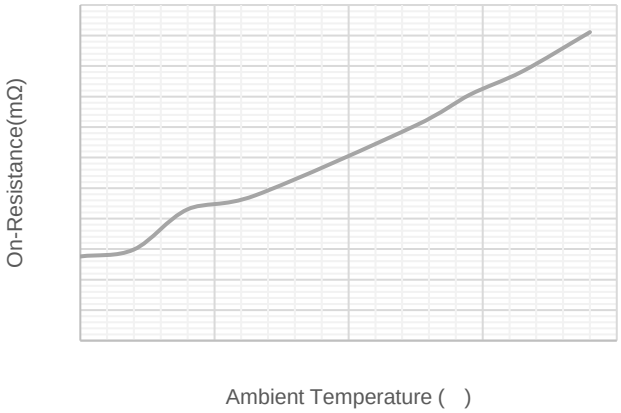


Figure 10. Channel-3 FET On-Resistance VS Temperature

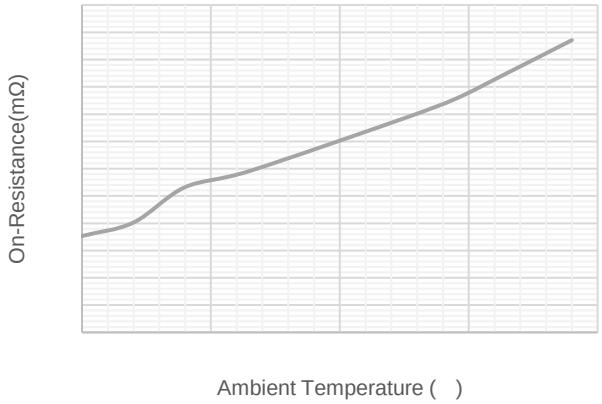


Figure 11. Channel-4 FET On-Resistance VS Temperature

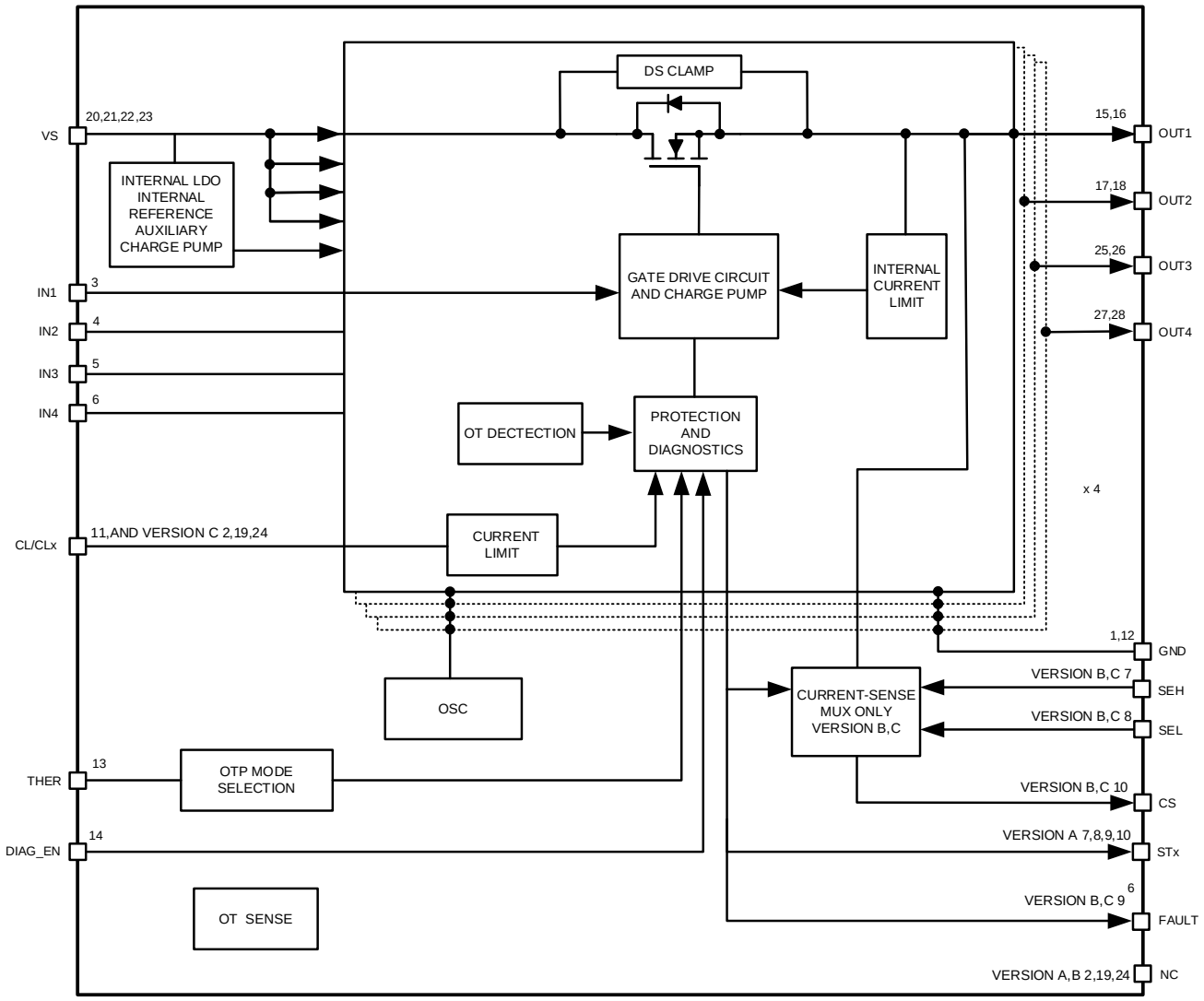


Figure 12. Functional Block Diagram

Overview

SCT44160 is a four-channel intelligent high-side switch that internally integrates a charge pump and four power N-MOSFETs. SCT44160 offers external adjustable threshold overcurrent protection functionality, with a typical value of 7A for internal current limiting to enhance design flexibility and system reliability. This device features comprehensive diagnostic functions and high-precision current sensing functions to achieve smart control of the load. Among SCT44160's three versions, Version A includes an open-drain digital output diagnostic mode. Version B provides current sensing analog output. Version C provides four external adjustment functions for overcurrent thresholds based on version B.

In Version A, an open-drain digital output is utilized, and the diagnostic output pin STx needs to be pulled down to the ground externally by providing a pull-up voltage of 3.3V or 5V to match the MCU. The abnormal status of each channel in version A can be reported separately to help the system quickly locate problematic channels.

Version B has a current sensing analog output, enabling the system to accurately determine the operational status of each channel. The integrated current mirror of the device provides a mirror current of $1/K_{CS}$ load current, which flows through the CS resistor and becomes a voltage signal to achieve analog output of load current. Version B can achieve the current information detection function for each channel through cyclic selection of SEH SEL pins. Additionally, in the event of an abnormality in a specific channel, the global diagnostic function of the Fault pin can be employed to pinpoint the problematic channel.

The diagnostic function of version C is consistent with version B, but version C can set four overcurrent thresholds separately. Four overcurrent thresholds can be reasonably set according to the application environment, further improving the flexibility and reliability of system design.

SCT44160 has a clamping function between the drain and source electrodes, which can effectively protect itself under inductive load conditions.

SCT44160 is an intelligent high-side switch suitable for applications where resistance, capacitance, and inductance loads can support most small load currents.

Adjustable Current Limit

SCT44160 has an adjustable high-precision current limitation mechanism. When the load current reaches the designated threshold, it rapidly internally controls the N-MOSFET gate voltage to clamp the output current to the set value and report faults. When overcurrent occurs, there is high power dissipation in the device. If the device heats up and triggers thermal shutdown, the current limit will be reduced to $I_{CL\ (TSD)}$ to reduce power dissipation on the device and further protect the device.

SCT44160 has two overcurrent protection thresholds, internal and external.

Internal current limitation, SCT44160 has a conventional value of 7A for internal integrated current limitation. When the CL/CLx pin is connected to the IC GND, the external current limitation becomes inactive, and protection is solely managed by the internal current limitation. This configuration is generally suitable for applications involving low VS voltage transient high current instances. At this point, there is a certain application risk when VS is under high voltage.

External adjustable current limit, SCT44160 can set the current limit threshold through an external R_{CL} resistor, which needs to be connected between CL and IC GND. Use Equation 1 to calculate the RCL resistance:

$$= \frac{\times}{\qquad} \tag{1}$$

Where

- V_{CL} is an internal reference value with a typical value of 0.8V
- K_{CL} is a typical value of 2500 for the load current sampling ratio

Accurate Current Sense

Version B and version C have high-precision current detection functions, which can accurately detect the real-time status of each channel, making it convenient for the system to accurately diagnose the status of each channel. Version B and version C internally integrate a current mirror to mirror the load current. The ratio between the load current and the mirror current is K_{CS}: 1, and the mirror current flows through the CS pin and an external ground resistor R_{CS}, generating a voltage signal to achieve load current detection. The current mirror is shared among all four channe

SEL pins for multi-channel current detection and fault report multiplexing, and select the corresponding channel of the CS pin to read whether the voltage of the CS pin is V

IC GND and the DIAG_EN or THER pin connected to external ground. Regardless of whether INx is high or low, the channels will be deactivated for protection.

Thermal Shutdown

Under extreme conditions like overcurrent, the device undergoes substantial power stress and heats up rapidly. SCT44160 incorporates two types of thermal protection: absolute thermal protection and relative thermal protection. These are designed to prevent rapid overheating of the device without protection.

When absolute overheating occurs, the thermal shutdown will be triggered, and the behavior after thermal shutdown can be determined by configuring THER:

1. When the THER pin is low, thermal shutdown enters automatic restart mode. After triggering the thermal shutdown, when $TJ<T_{SD}-T_{HYS}$, the output will recover, but the current limit threshold will be reduced to 40% of the design value, reducing power stress and enhancing protection. When $TJ<T_{SD\_RST}$ or related INx pin restart thermal fault signal will be cleared.
2. When THER pin is high, thermal shutdown enters latch mode. After the thermal shutdown, the output will be locked, and the channel will be deactivated. The thermal fault signal from the relevant INx pin is cleared, or switching the THER pin level to ground will transition the thermal shutdown into automatic restart mode.

Inductive-Load Switching-Off Clamp

When disconnecting the inductive load, the output will be pulled negative due to the influence of the induced electromotive force. At this time, the VS voltage is still positive, and excessive output negative voltage may cause power MOSFET voltage breakdown. To protect the device, the SCT44160 internally integrates a voltage clamp function, namely $V_{DS\ (clamp)}$. When the output negative voltage is too large, the voltage between V_{VS} and V_{OUTx} will be clamped to $V_{DS\ (clamp)}$ to protect the power MOSFET When the energy of the inductive load is too large, it is recommended to use the method shown in Figure 13 for further protection

Protection for Loss of Power Supply

There is no risk for resistive or capacitive loads when the input power supply suddenly disconnects. However, for inductive loads, sudden changes in inductance current will generate induced electromotive force. It is recommended to add a GND network or external freewheeling diode to prevent excessive energy from damaging the chip. Join GND network THE and DIAG_ EN cannot be grounded to prevent ground failure error reporting.

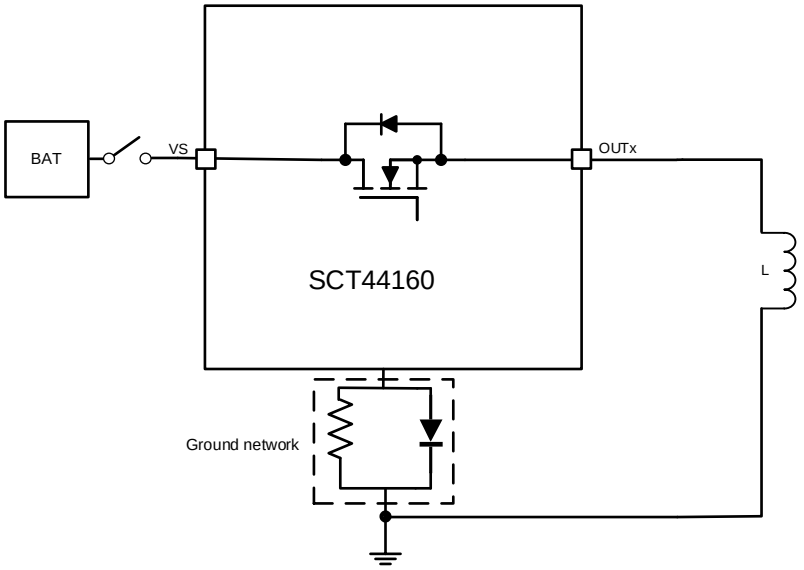


Figure 14. Ground Network Power Loss Protection

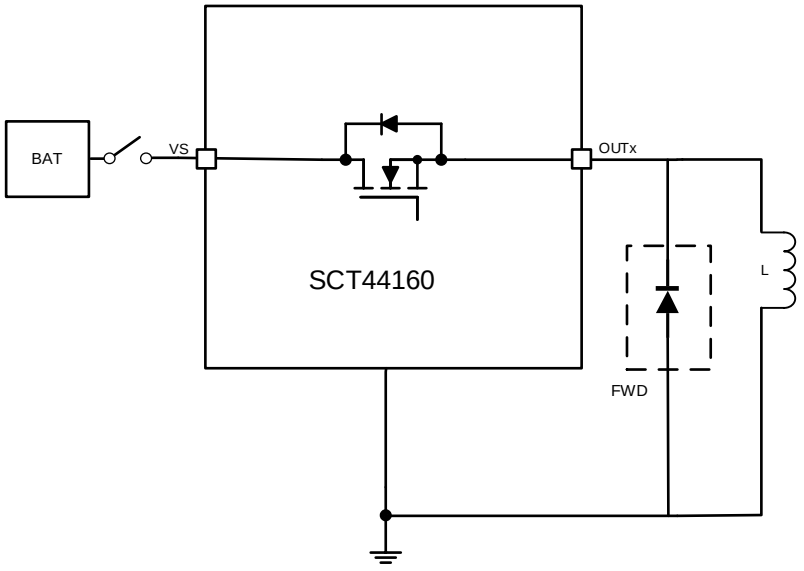


Figure 15. The Freewheeling Diode Power Loss Protection

Reverse-Current Protection

When there is an input short circuit, the reverse current flows to the input through the body diode, and when the input polarity is reversed, the reverse current flows to the input through GND and the body diode. Since the current-handling capacity of the GND pin is limited, for device protection, it's advisable to include a reverse

protection diode at the input or incorporate it into the GND network. When a reverse protection diode is added to the input, both the load and the device are protected.

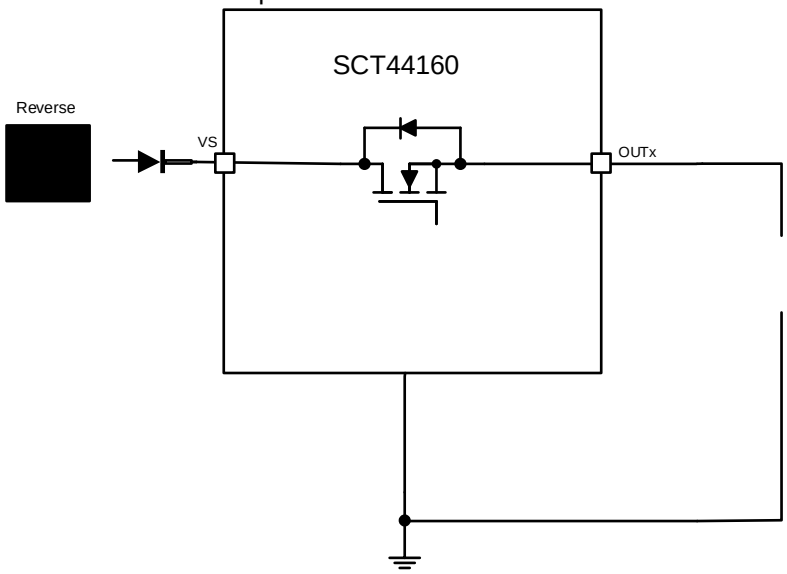


Figure 16. Anti Reverse Diode Power Reverse Protection

By adding to the GND network, the current flowing into IC GND will be limited, thus protecting the device.

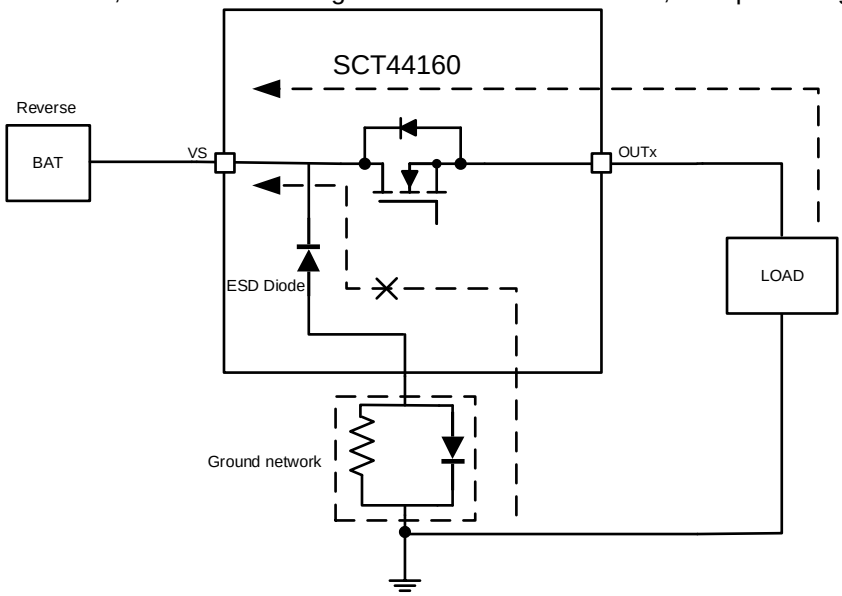


Figure 17. Ground Network Power Reverse Protection

MCU I/O Protection

In some extreme cases, such as inductive load input disconnection, negative voltage pulses may appear in the IC GND relative to the system ground. To protect the MCU and the device, it is recommended to connect a series resistor between the MCU and the SCT44160 logic control pin.

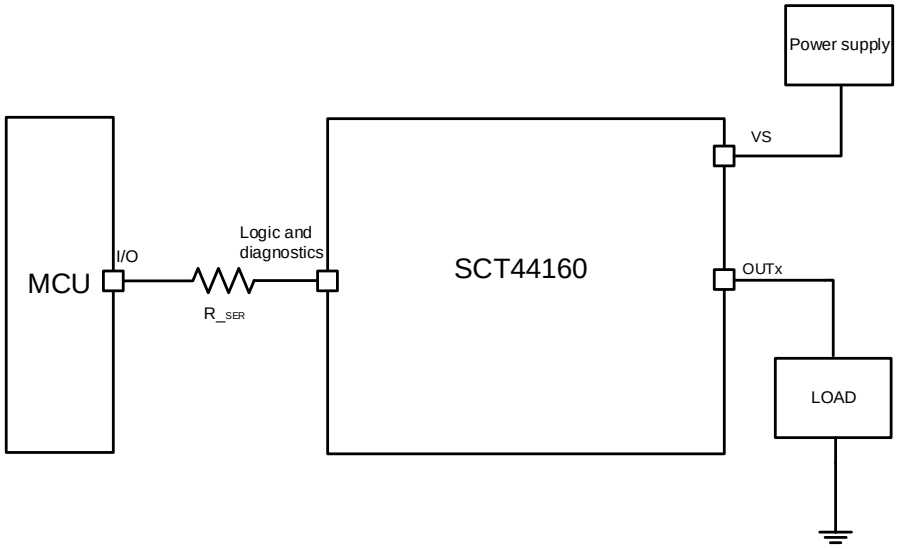


Figure 18. MCU I/O Protection

Typical Application

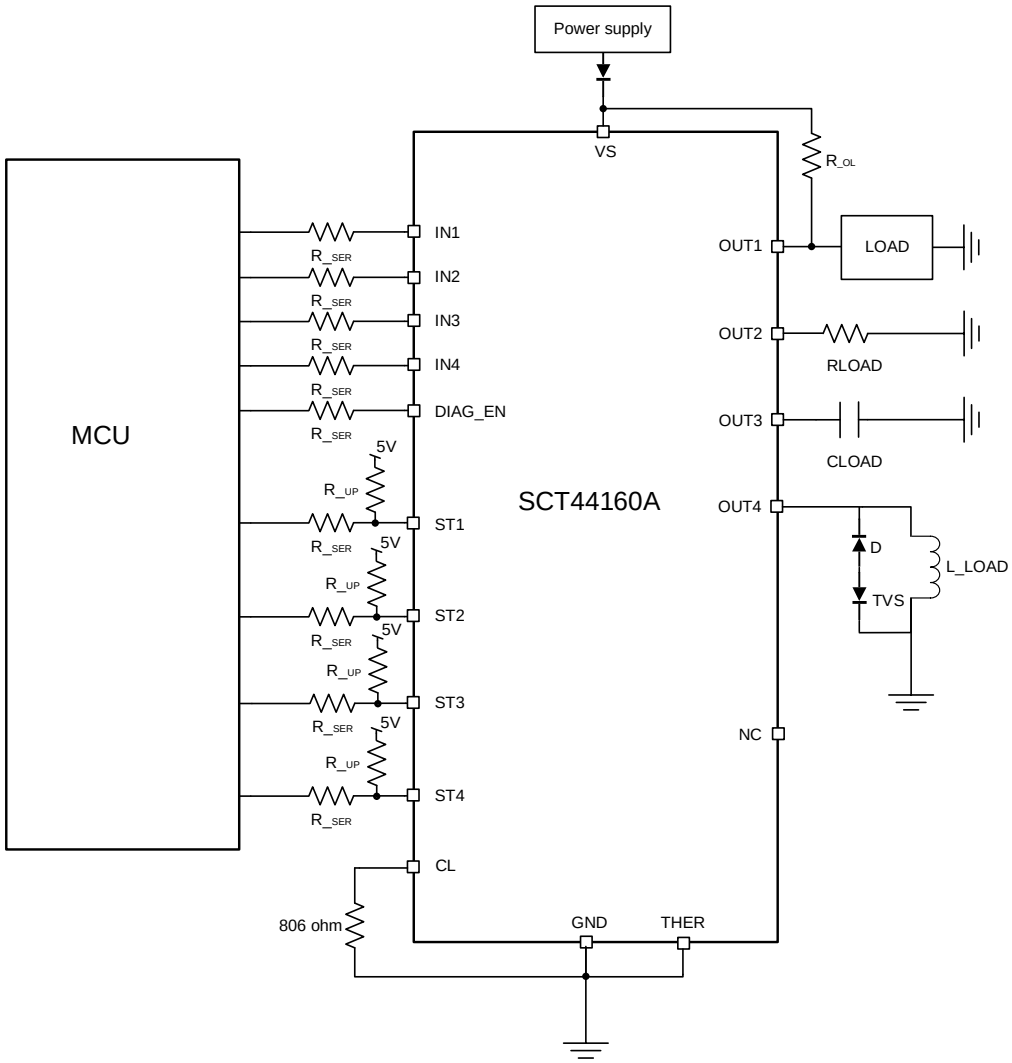


Figure 19. Version A Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	13.5V Normal 8V to 18V
Load Current	Typical 1A
Current Limit	2.5A
MCU Voltage	5V

Typical Application (continued)

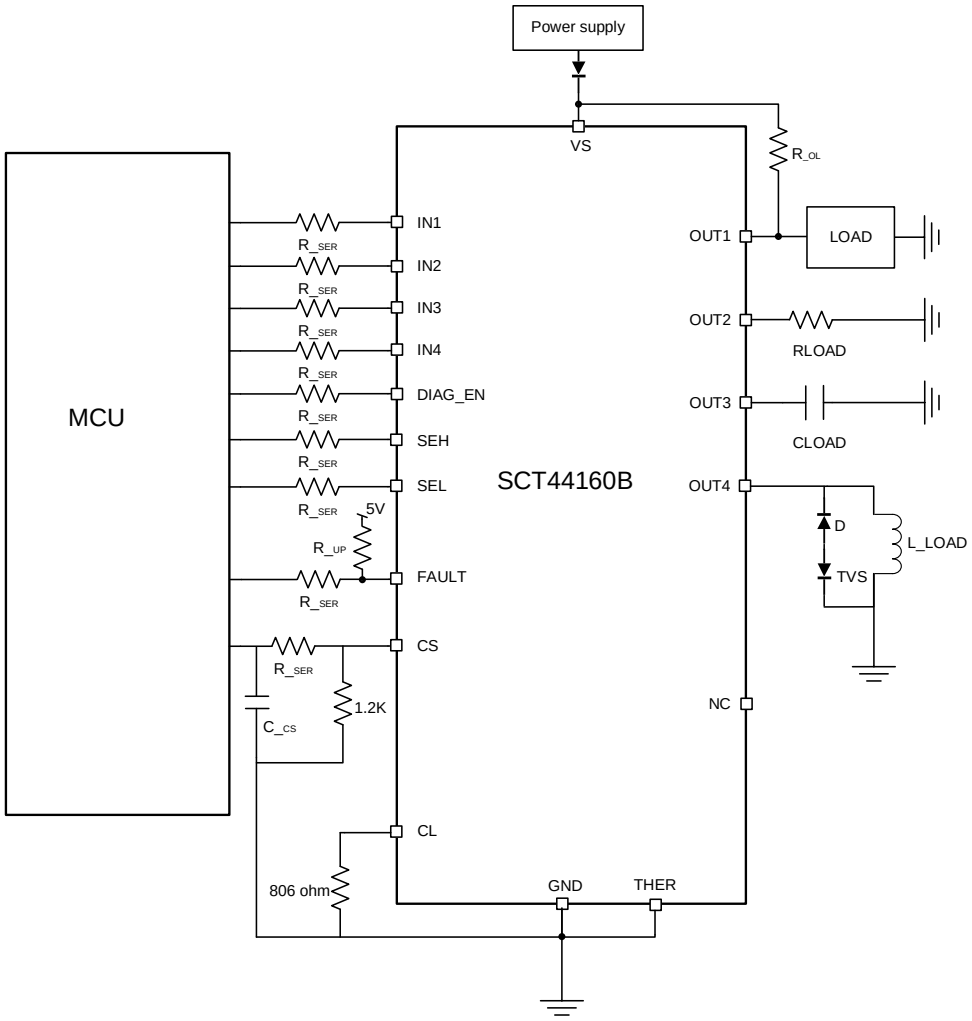


Figure 20. Version B Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	13.5V Normal 8V to 18V
Load Current	Typical 1A
Current Limit	2.5A

Typical Application (continued)

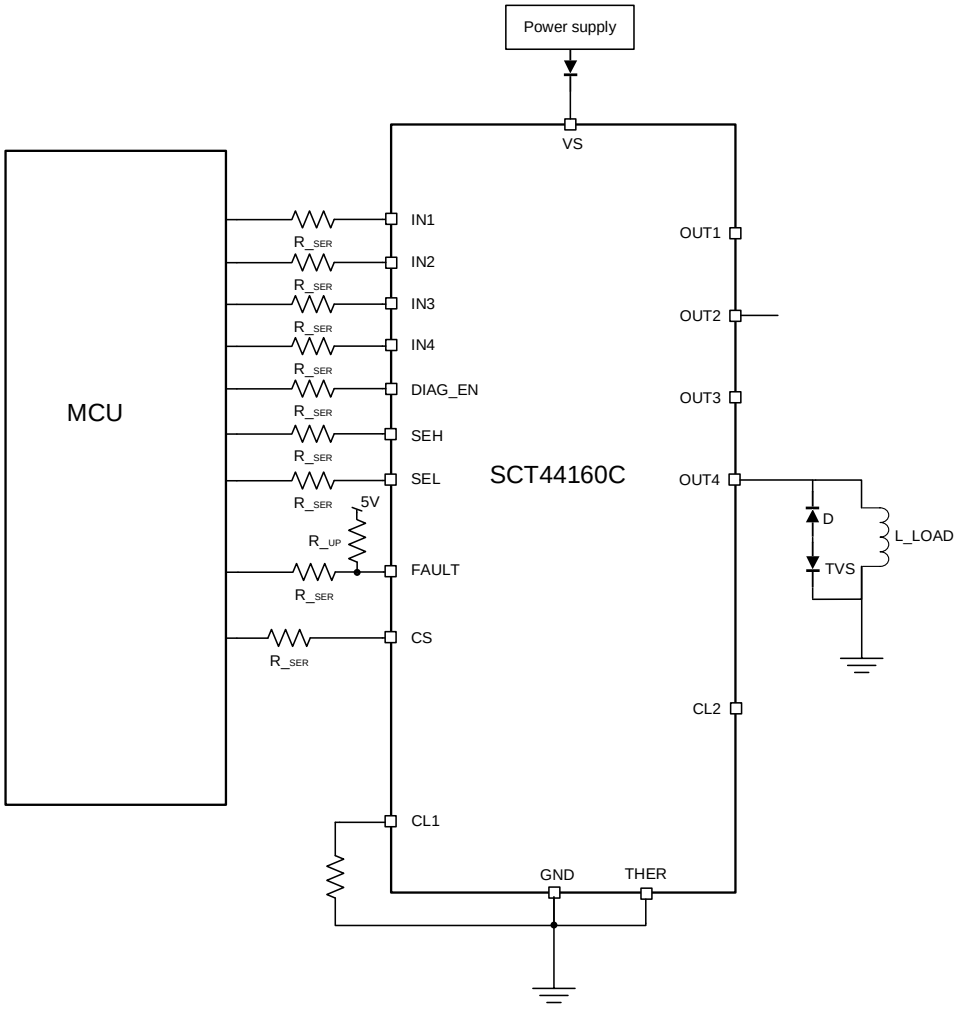


Figure 21. Version C Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	13.5V Normal 8V Î M

Application Waveforms

V_{VS}=13.5V, unless otherwise noted

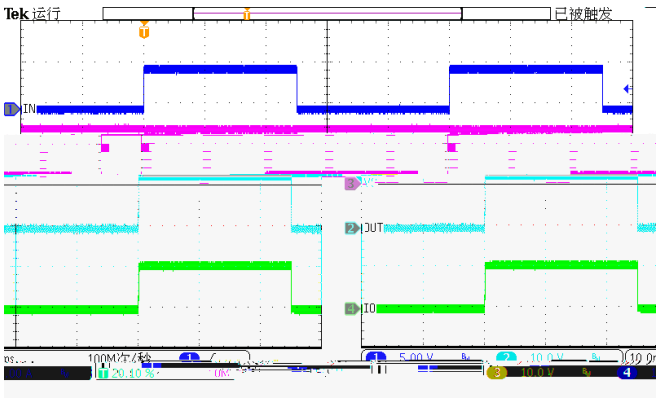


Figure 22. IN Toggle resistive load 1A

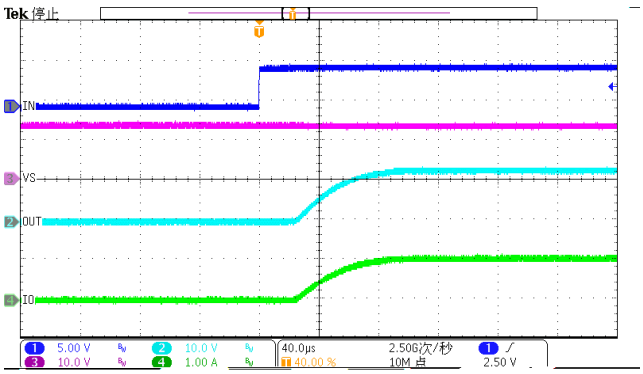


Figure 23. IN On resistive load 1A

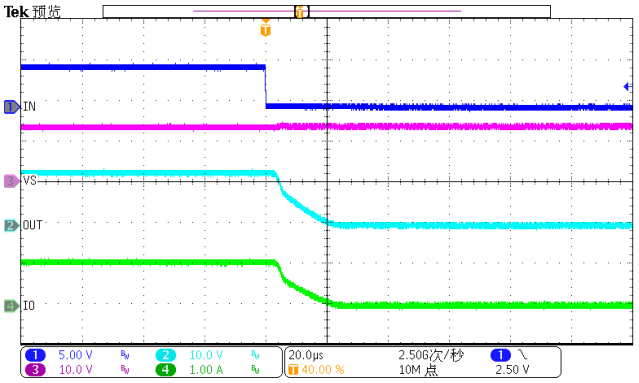


Figure 24. IN Off resistive load 1A

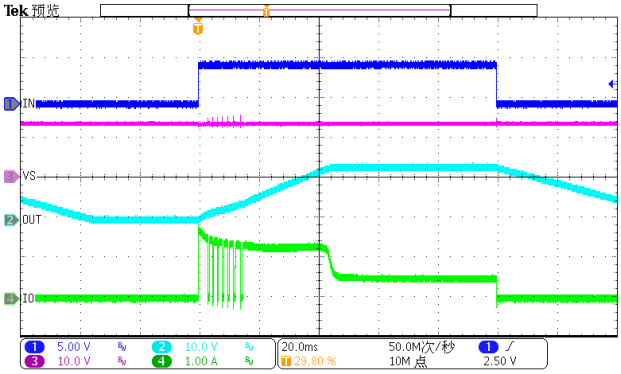


Figure 25. IN Toggle capacitive load C=2.2mF

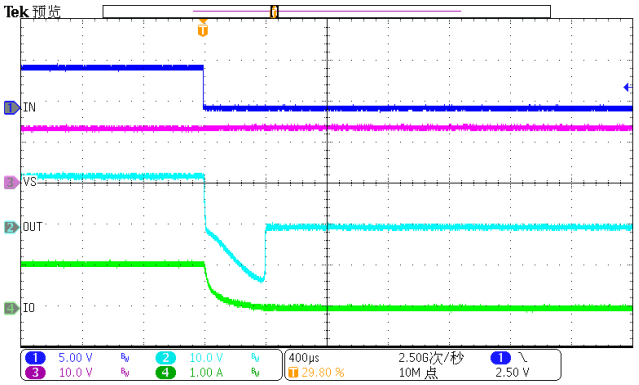


Figure 26. IN Off Inductive load L=8mH series resistor=13.5Ω

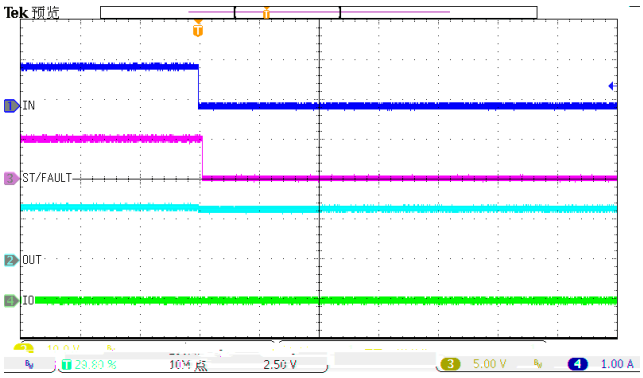


Figure 27. Open-load detection

Application Waveforms(continued)

V_{VS}=13.5V, unless otherwise noted

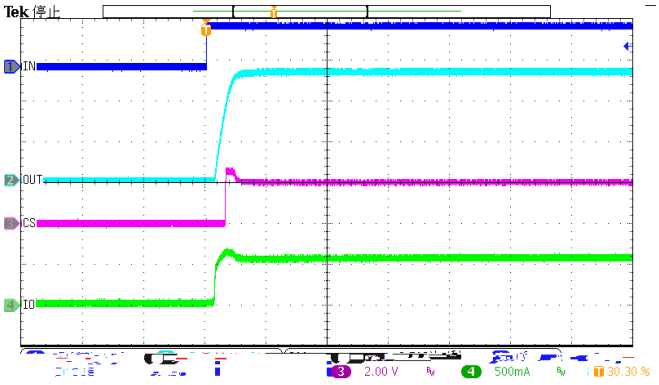


Figure 28. IN On current sense load=0.5A

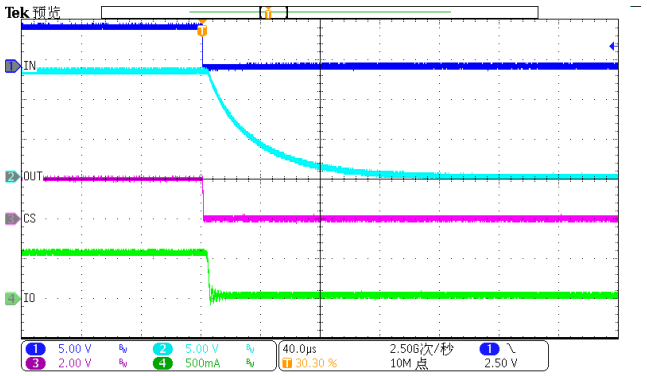


Figure 29. IN Off current sense load=0.5A

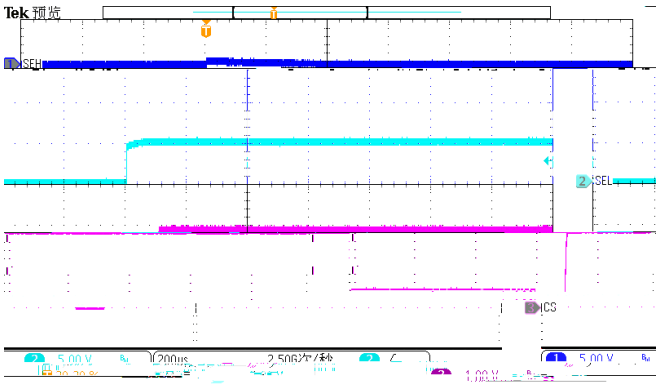


Figure 30. Current sense CH1-CH2

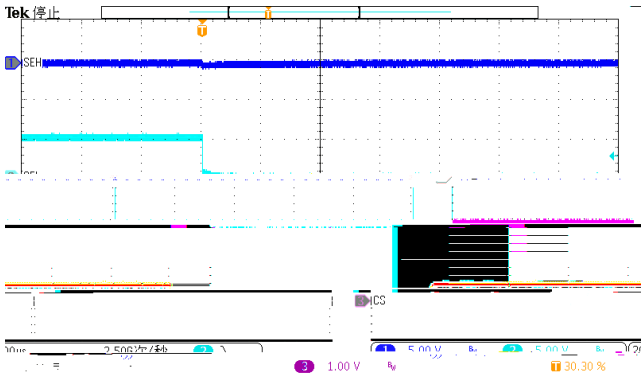


Figure 31. Current sense CH2-CH1

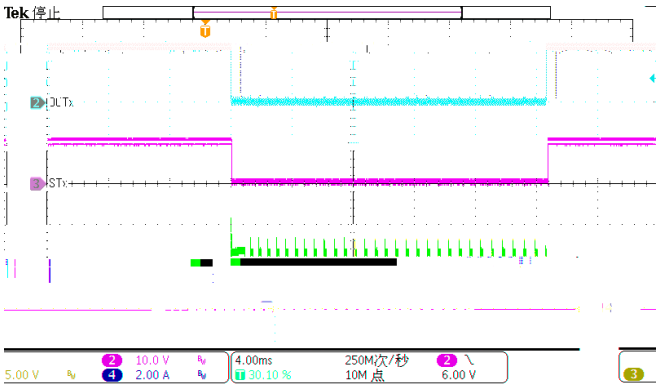


Figure 32. Overcurrent detection for version A

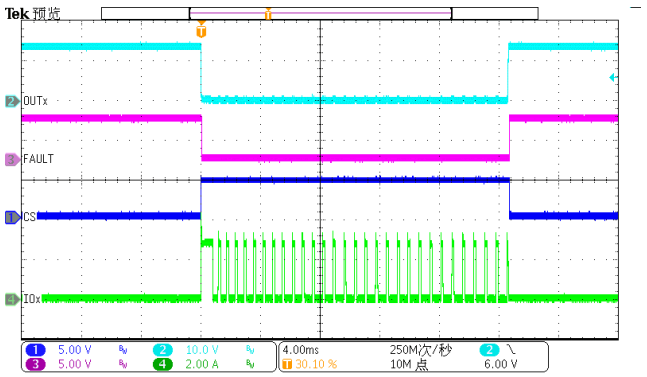


Figure 33. Overcurrent detection for version B/C

Layout Guideline

The PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

1. Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
2. More vias should be placed below the device Thermal PAD to further improve heat transfer.
3. R_{CL} should be connected to IC GND.

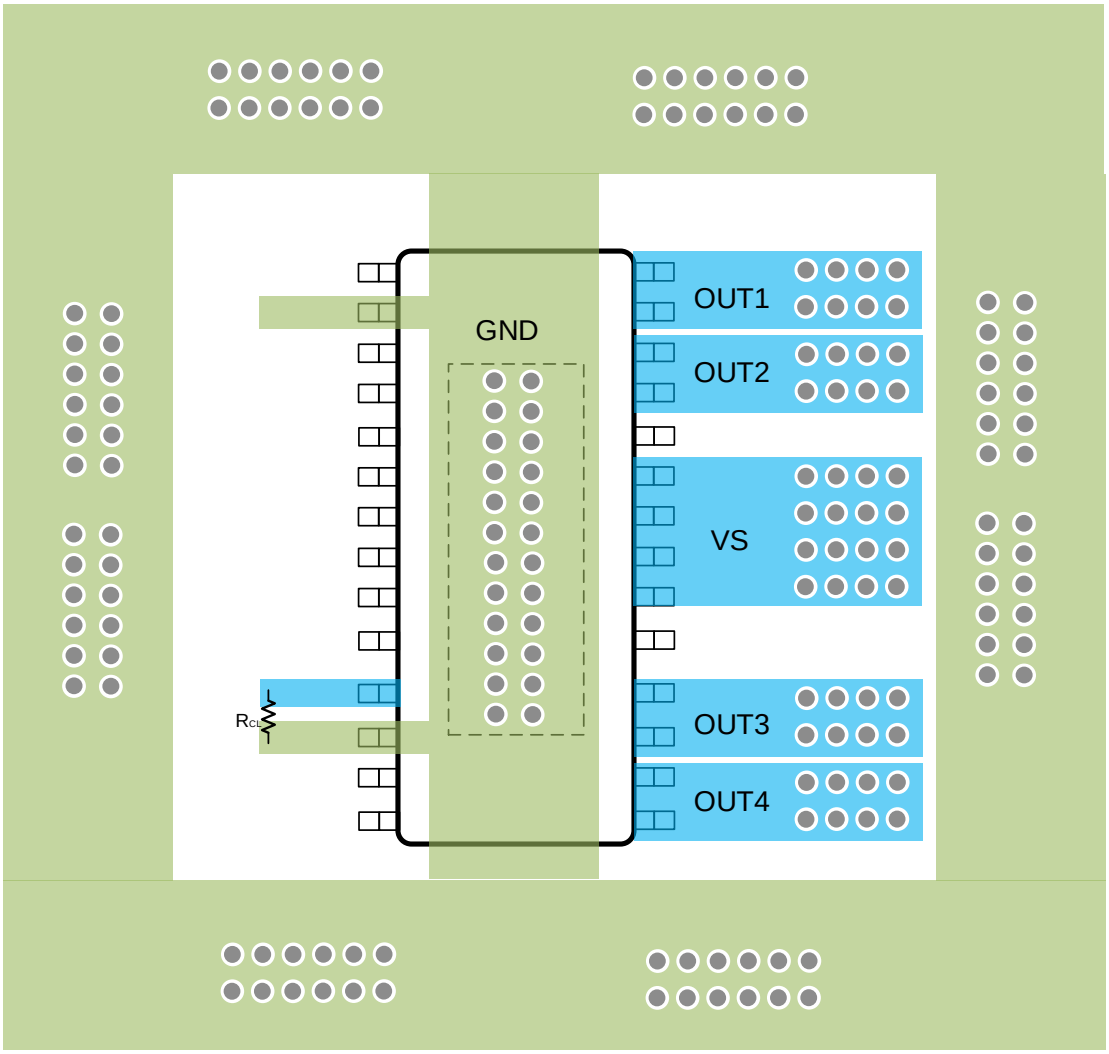
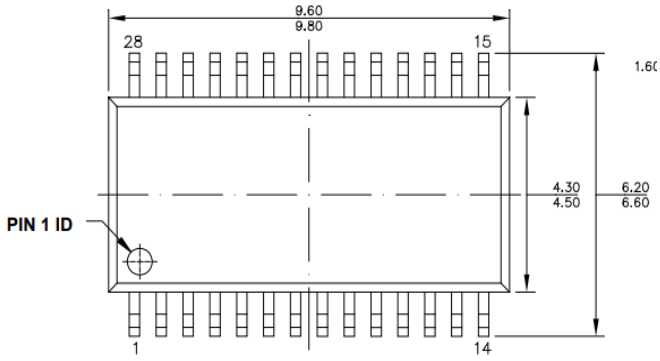
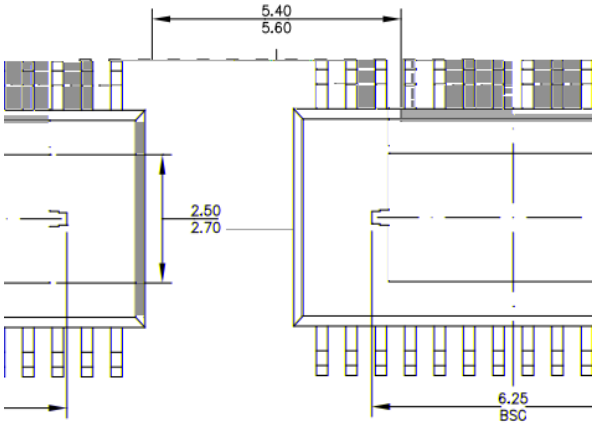


Figure 34. Without a GND Network PCB Layout

Figure 35. With a GND Network PCB Layout

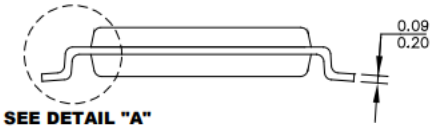


TOP VIEW

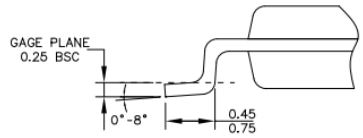


BOTTOM VIEW

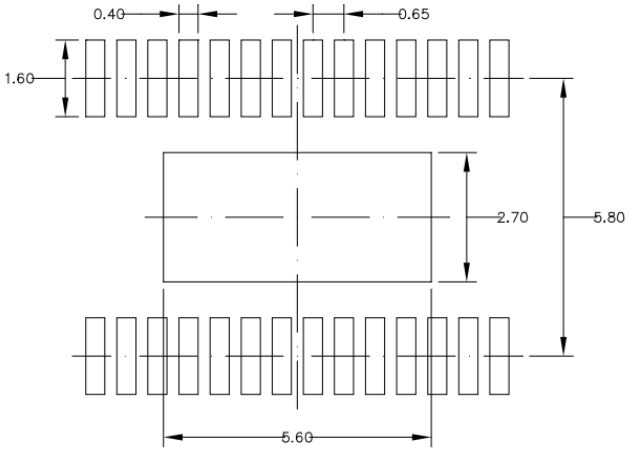
FRONT VIEW



SIDE VIEW



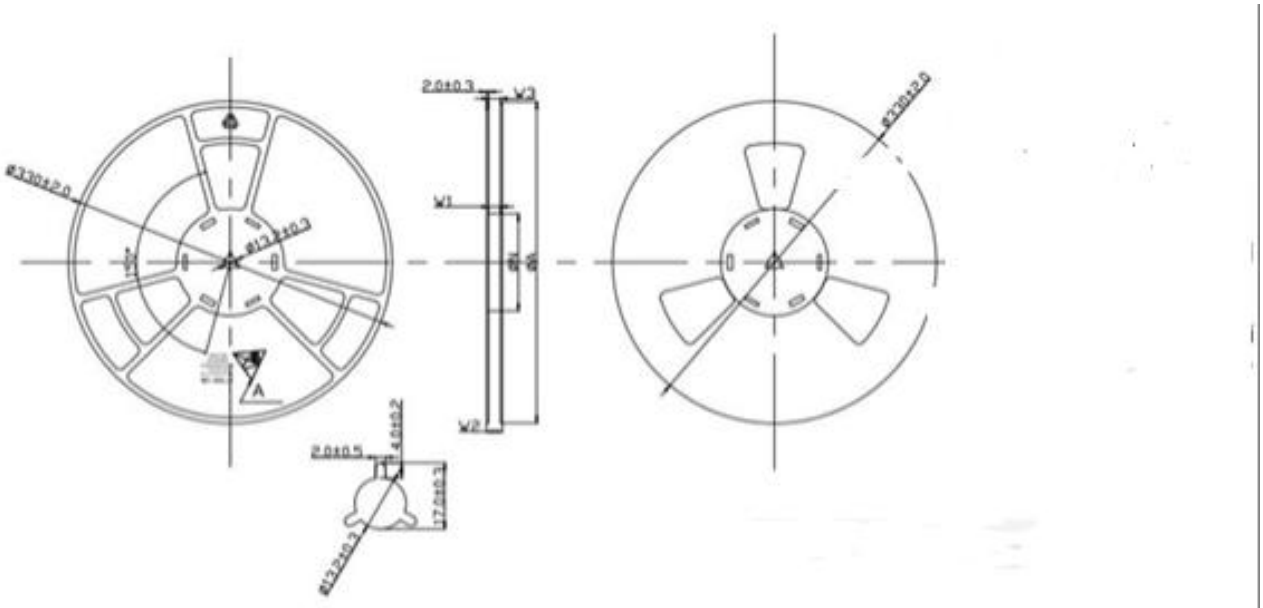
DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS..
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3. PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5. DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6. DRAWING IS NOT TO SCALE.



PRODUCT SPECIFICATIONS					
TYPE WIDTH	ØA	ØN	W1(min)	W2(Max)	W3(Min)
16MM	330±2.0	100±1.0	16.4	22.4	15.9/19.4